

EASYIO

**EASY INPUT AND OUTPUT PLATFORM
FOR
MATLAB/SIMULINK**

Quick Reference

release 2.1

May 1, 2016

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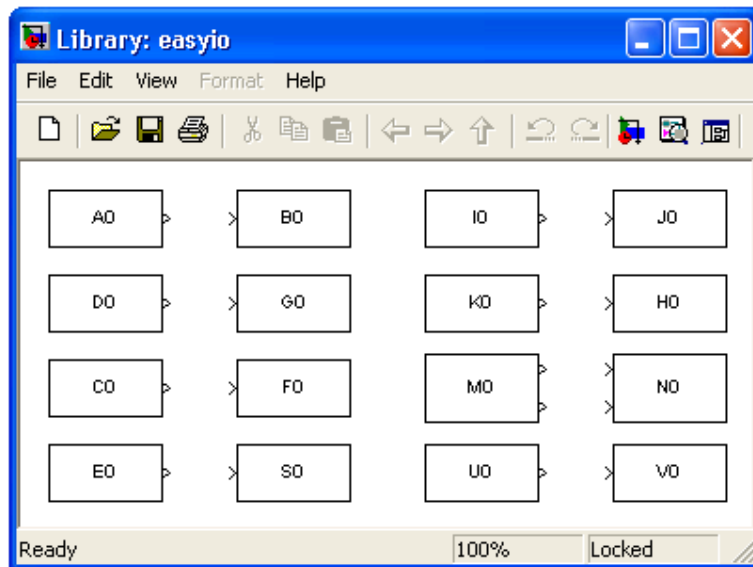
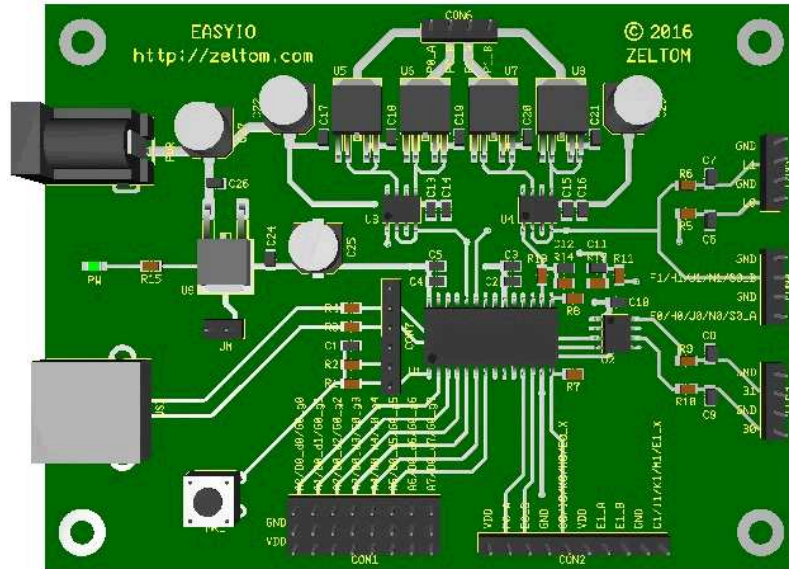
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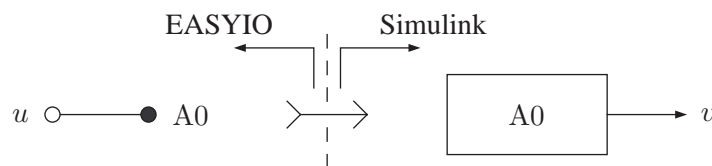
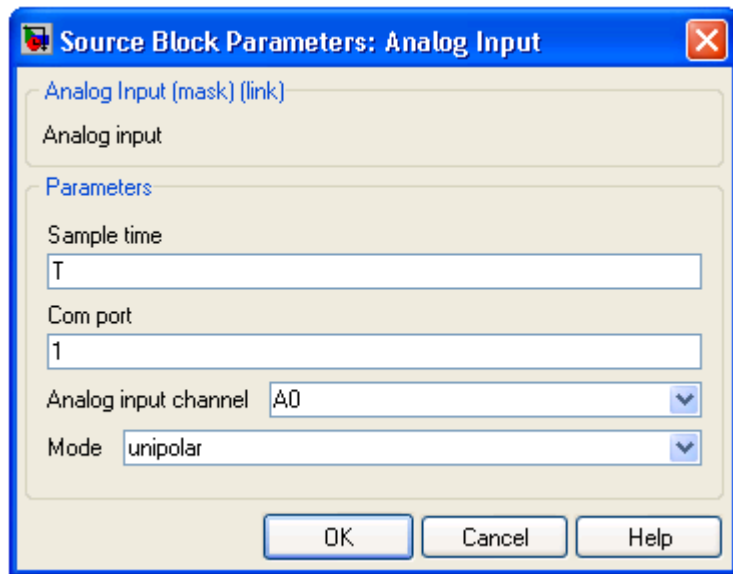
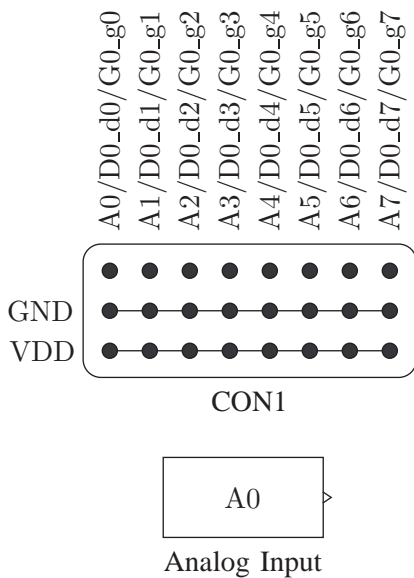
Belleville, MI 48111

USA



1. Analog Input

- 8 analog input channels A0 – A7
- Board input: 0 – 5 V analog signal
- Block output: unipolar or bipolar amplitude of analog signal
- Resolution: 12 bit
- Sampling rate: 28.7891 kHz (internal)
- 610.3516 μV maximum unipolar amplitude quantization error and 1220.7031 μV maximum bipolar amplitude quantization error

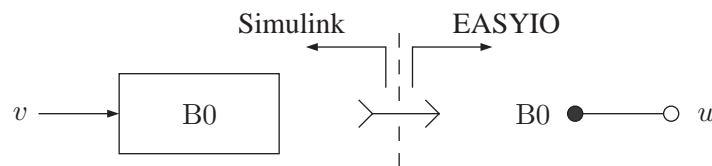
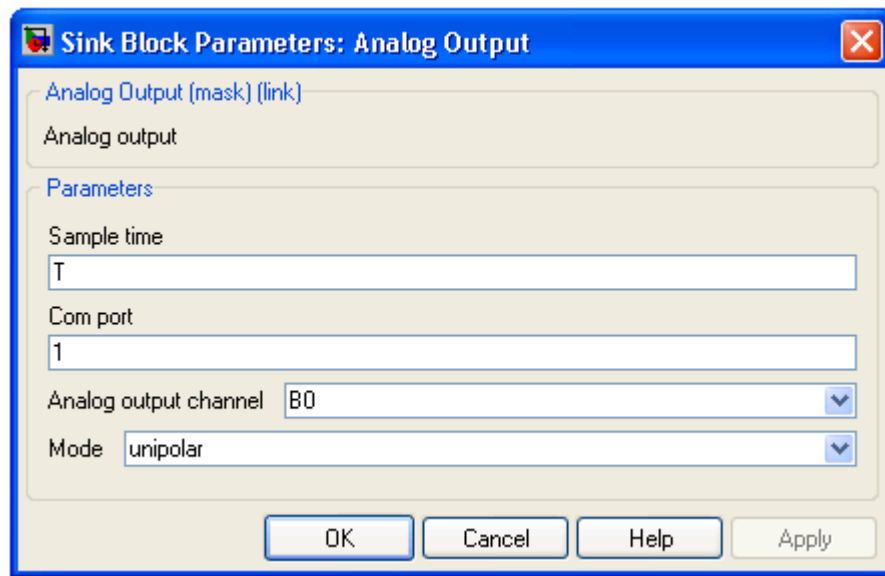
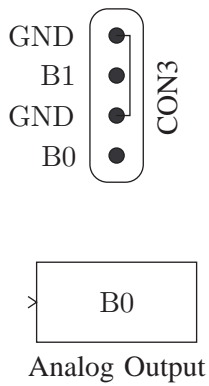


$$\text{unipolar mode} \Rightarrow v \approx \begin{cases} 5, & u \geq 5 \\ u, & 0 < u < 5 \\ 0, & u \leq 0 \end{cases}$$

$$\text{bipolar mode} \Rightarrow v \approx \begin{cases} +5, & u \geq 5 \\ 2u - 5, & 0 < u < 5 \\ -5, & u \leq 0 \end{cases}$$

2. Analog Output

- 2 analog output channels B0 – B1
- Block input: unipolar or bipolar amplitude of analog signal
- Board output: 0 – 5 V analog signal
- Resolution: 12 bit
- Settling time: 4.5 μ s
- 500.0000 μ V maximum unipolar amplitude interpolation error and 1000.0000 μ V maximum bipolar amplitude interpolation error

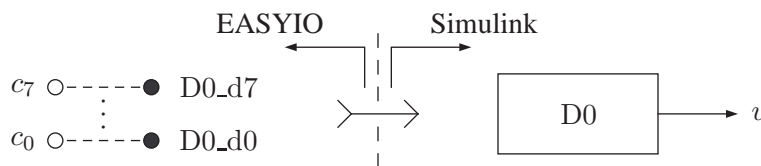
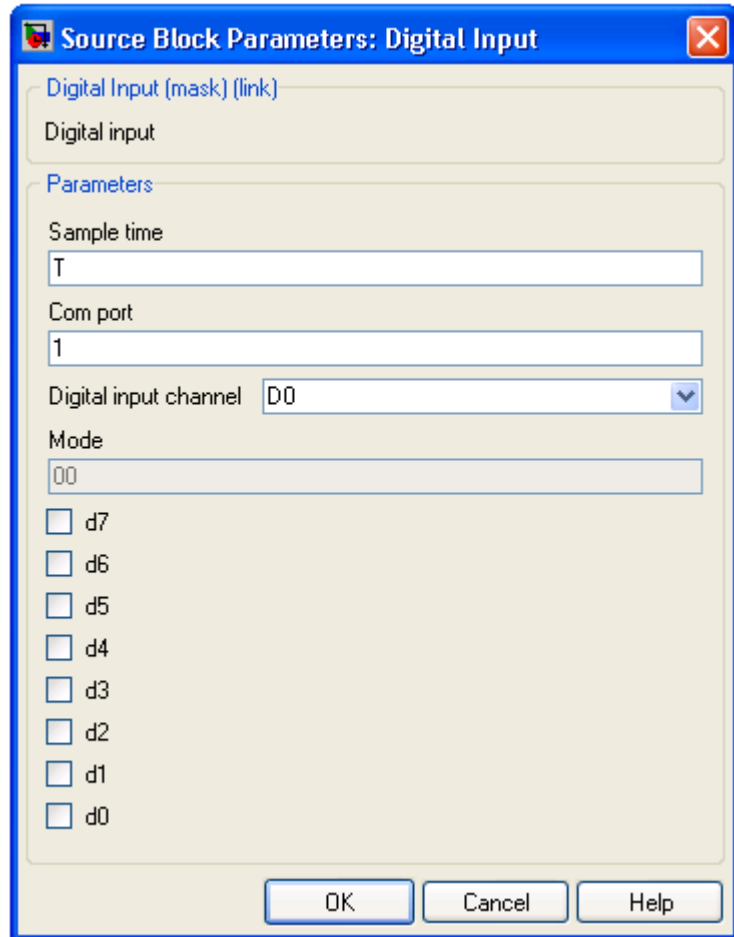
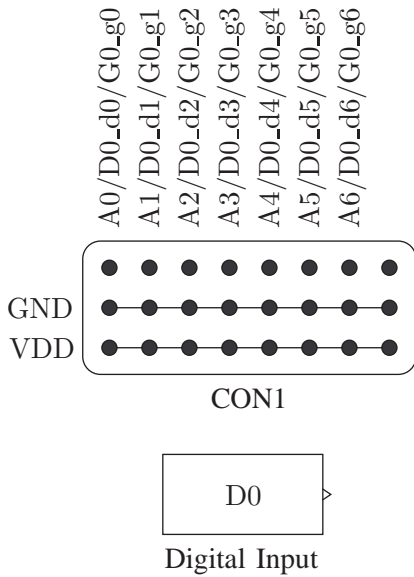


$$\text{unipolar mode} \Rightarrow u \approx \begin{cases} 4.096, & v \geq 4.096 \\ v, & 0 < v < 4.096 \\ 0, & v \leq 0 \end{cases}$$

$$\text{bipolar mode} \Rightarrow u \approx \begin{cases} 4.096, & v \geq +4.096 \\ v/2 + 4.096/2, & -4.096 < v < +4.096 \\ 0, & v \leq -4.096 \end{cases}$$

3. Digital Input

- 1 digital input channel D0 with 8 digital input lines D0_d0 – D0_d7
- Board input: 0 – 5 V digital signal
- Block output: decimal representation of digital signal

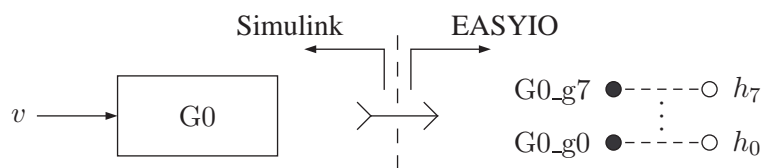
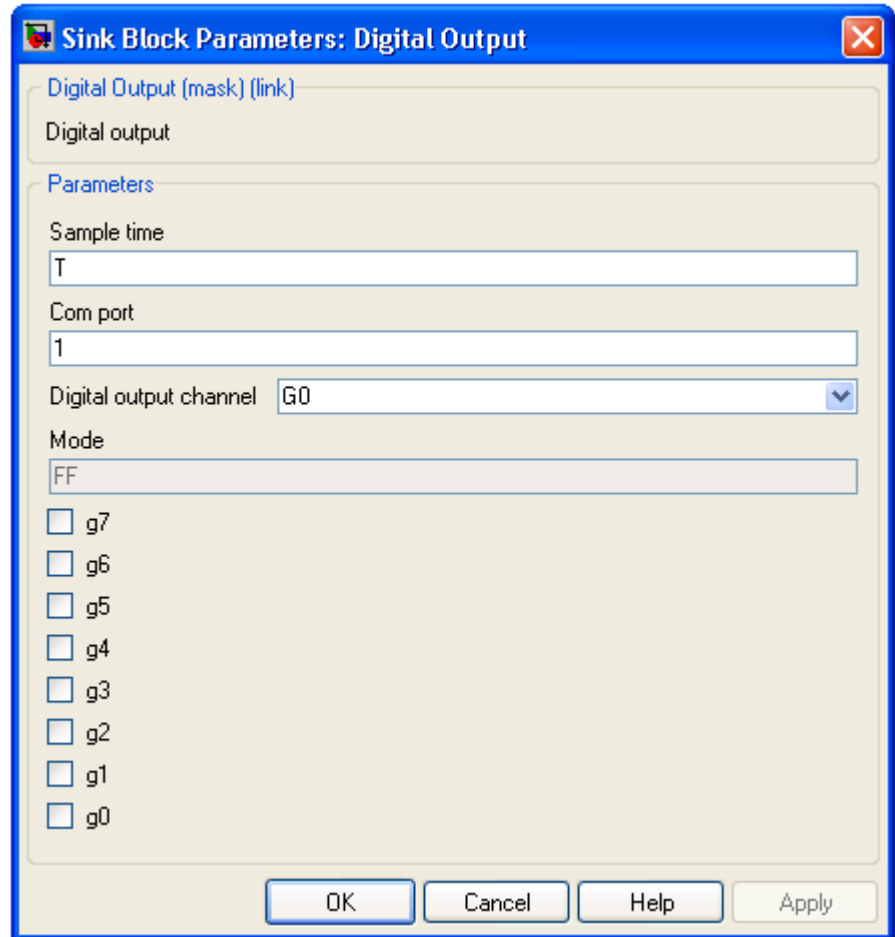
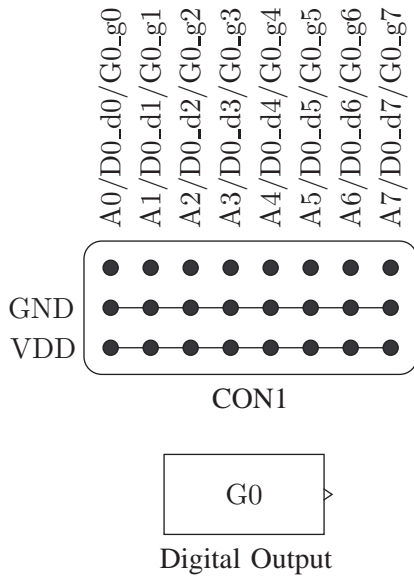


$$v = 128 d_7 + 64 d_6 + 32 d_5 + 16 d_4 + 8 d_3 + 4 d_2 + 2 d_1 + 1 d_0$$

$$d_i = \begin{cases} c_i (1 \text{ or } 0), & \text{Ai is not used and D0_di is used (di is checked)} \\ 0, & \text{Ai is used, or Ai, D0_di and G0_gi are not used} \\ h_i (1 \text{ or } 0), & \text{Ai and D0_di are not used, but G0_gi is used with output } h_i \end{cases}$$

4. Digital Output

- 1 digital output channel G0 with 8 digital output lines G0_g0 – G0_g7
- Block input: decimal representation of digital signal
- Board output: 0 – 5 V digital signal

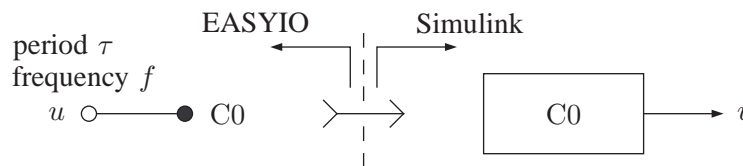
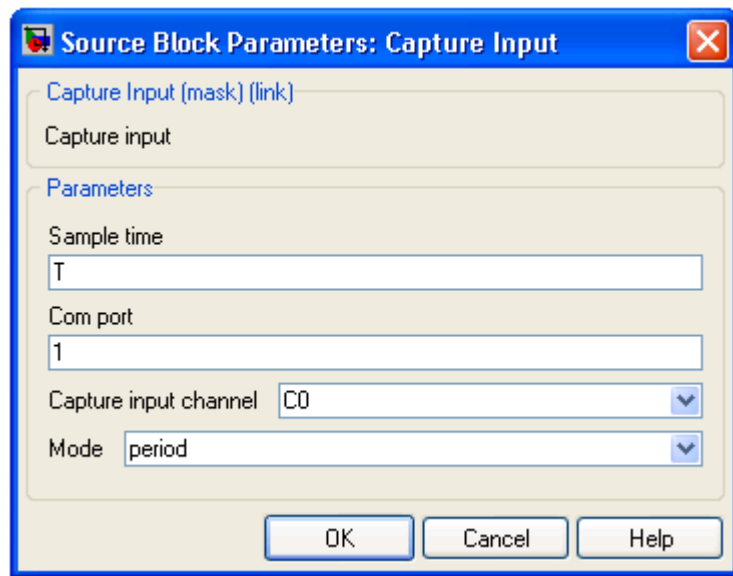
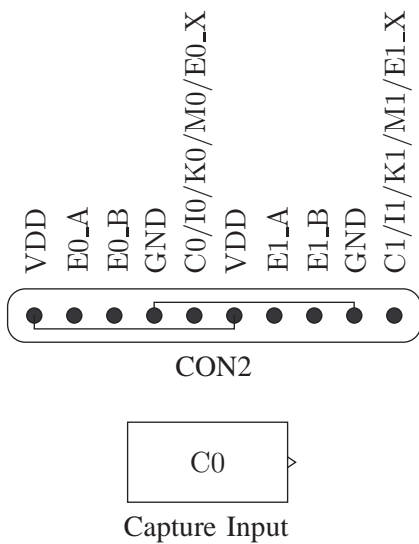


$$128 g_7 + 64 g_6 + 32 g_5 + 16 g_4 + 8 g_3 + 4 g_2 + 2 g_1 + 1 g_0 = v \& 0 \times 00FF$$

$$h_i = \begin{cases} g_i \text{ (1 or 0),} & \text{Ai and D0_di are not used, and G0_gi is used (gi is checked)} \\ \text{(analog input),} & \text{Ai is used, or Ai, D0_di and G0_gi are not used} \\ c_i \text{ (1 or 0),} & \text{Ai is not used and D0_di is used with input } c_i \end{cases}$$

5. Capture Input

- 2 capture input channels C0 – C1
- Board input: 0 – 5 V digital signal
- Block output: period or frequency of digital signal
- Resolution: 16 bit
- Accuracy: $8.6839 \mu\text{s}$
- $8.6839 \mu\text{s}$ maximum period quantization error and $f - 115156.25 / \lfloor 115156.25 / f \rfloor$ Hz maximum frequency quantization error (f is the actual input frequency)

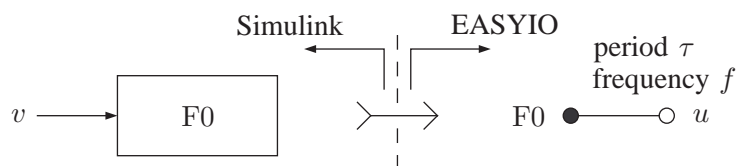
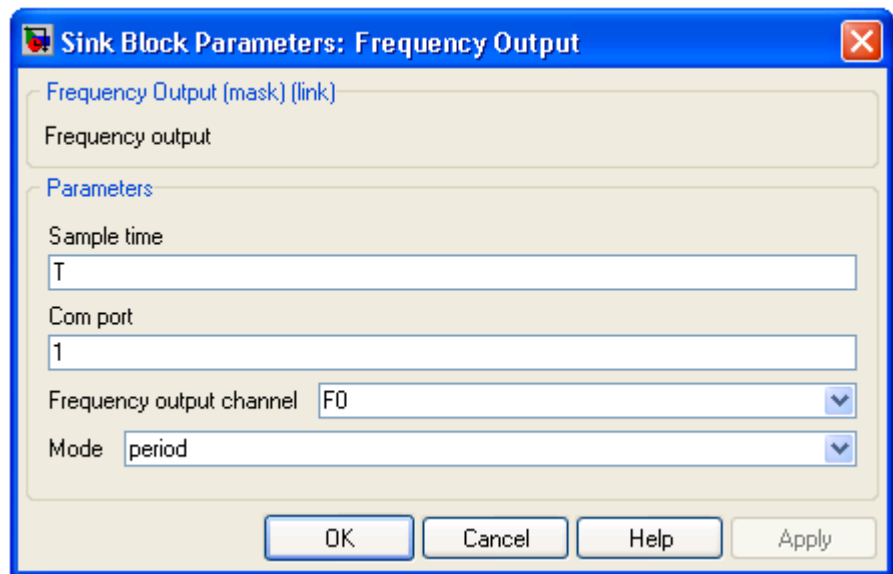
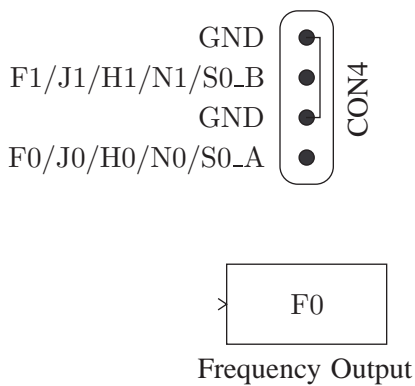


$$\text{period mode} \Rightarrow v \approx \begin{cases} 569.0963 \times 10^{-3}, & \tau \geq 569.0963 \times 10^{-3} \\ \tau, & 34.7354 \times 10^{-6} < \tau < 569.0963 \times 10^{-3} \\ 34.7354 \times 10^{-6}, & \tau \leq 34.7354 \times 10^{-6} \end{cases}$$

$$\text{frequency mode} \Rightarrow v \approx \begin{cases} 28789.0625, & f \geq 28789.0625 \\ f, & 1.7572 < f < 28789.0625 \\ 1.7572, & f \leq 1.7572 \end{cases}$$

6. Frequency Output

- 2 frequency output channels F0 – F1
- Block input: period or frequency of digital signal
- Board output: 0 – 5 V digital signal
- Resolution: 16 bit
- Accuracy: 8.6839 μ s
- 8.6839 μ s maximum period interpolation error and $f - 115156.25/[115156.25/f]$ Hz maximum frequency interpolation error (f is the desired output frequency)

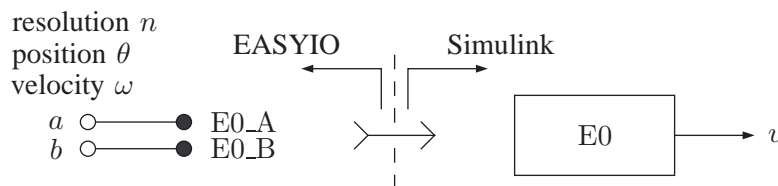
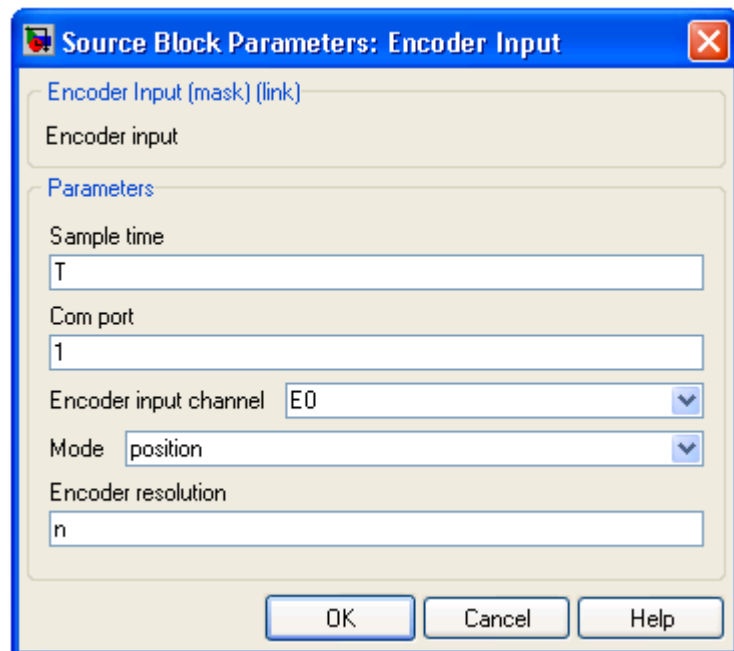
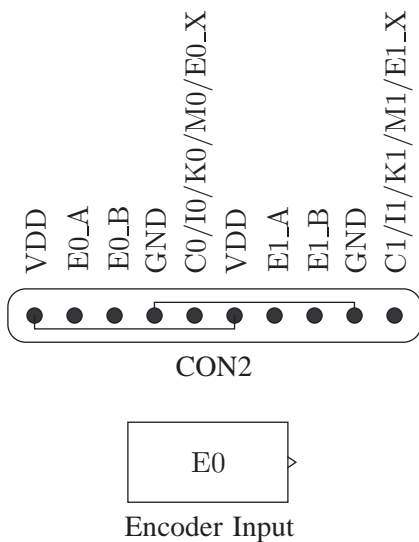


$$\text{period mode} \Rightarrow \tau \approx \begin{cases} 569.0963 \times 10^{-3}, & v \geq 569.0963 \times 10^{-3} \\ v, & 34.7354 \times 10^{-6} < v < 569.0963 \times 10^{-3} \\ 34.7354 \times 10^{-6}, & v \leq 34.7354 \times 10^{-6} \end{cases}$$

$$\text{frequency mode} \Rightarrow f \approx \begin{cases} 28789.0625, & v \geq 28789.0625 \\ v, & 1.7572 < v < 28789.0625 \\ 1.7572, & v \leq 1.7572 \end{cases}$$

7. Encoder Input

- 2 encoder input channels E0 – E1 with quadrature inputs E0_A, E0_B – E1_A, E1_B
- Board input: 0 – 5 V digital encoder signals
- Block output: position or velocity of encoder
- Resolution: 16 bit per sampling interval
- Scan rate: 307.0833 kHz
- $\pi/2/n$ rad maximum position quantization error and $153541.6667 \pi/n$ rad/s maximum measurable angular speed (n is the encoder resolution)

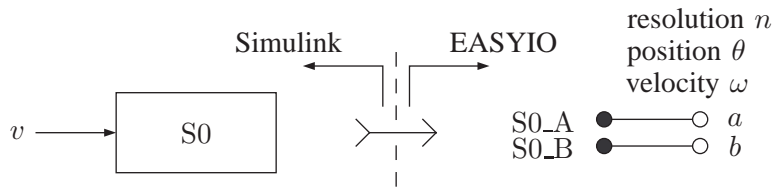
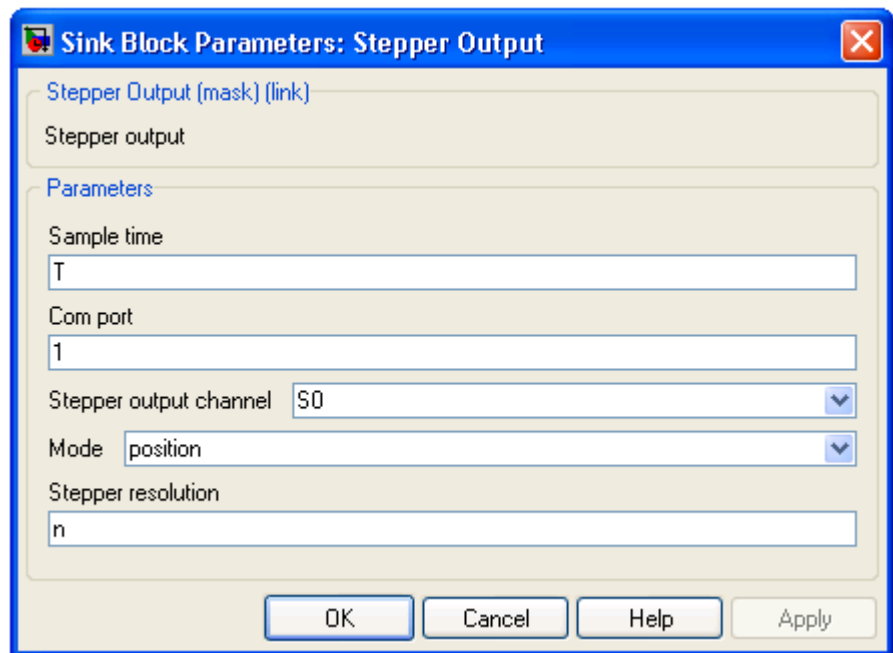
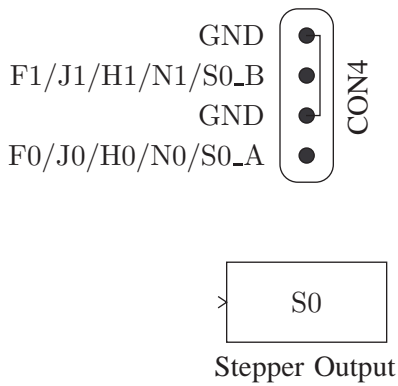


position mode $\Rightarrow v \approx \theta$

velocity mode $\Rightarrow v \approx \omega$

8. Stepper Output

- 1 stepper output channel S0 with quadrature outputs S0_A, S0_B
- Block input: position or velocity of stepper
- Board output: 0 – 5 V digital stepper signals
- Resolution: 16 bit per sampling interval
- Update rate: 28.7891 kHz
- $\pi/2/n$ rad maximum position interpolation error and $899.6582\pi/n$ rad/s maximum achievable angular speed (n is the stepper resolution)

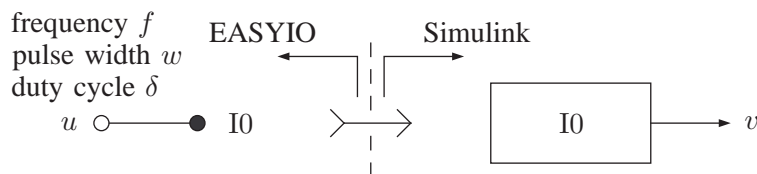
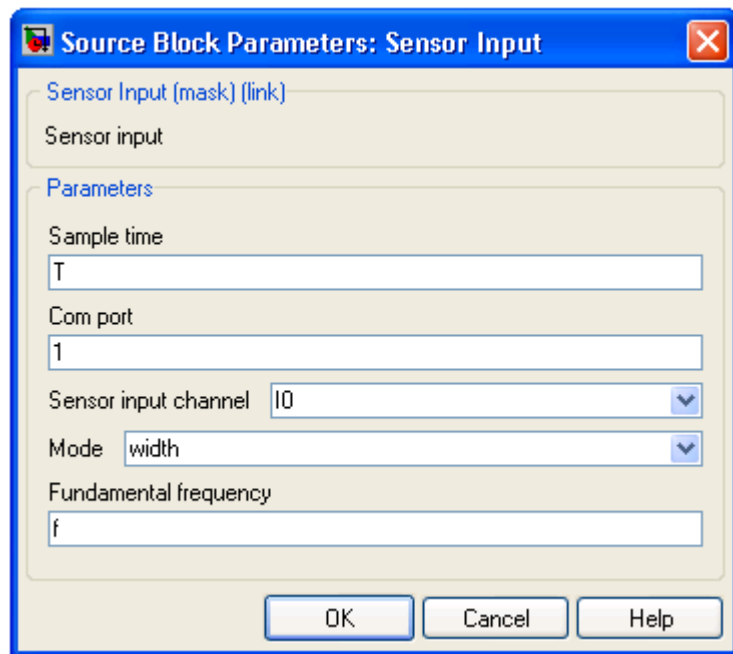
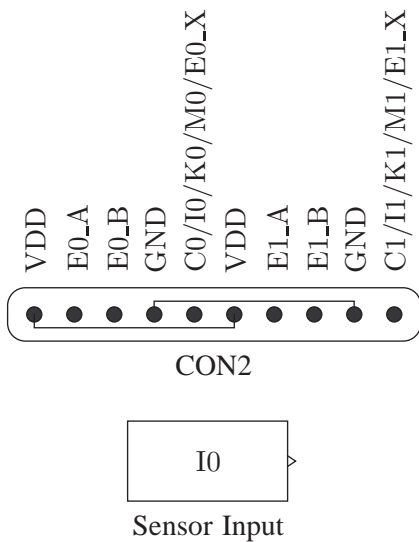


position mode $\Rightarrow \theta \approx v$

velocity mode $\Rightarrow \omega \approx v$

9. Sensor Input

- 2 sensor input channels I0 – I1
- Board input: 0 – 5 V digital signal
- Block output: pulse width or duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $7.0287 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$
- $2.1710 \mu\text{s}$ maximum pulse width quantization error and $2.1710 \times 10^{-6} f$ maximum duty cycle quantization error (f is the actual input frequency)

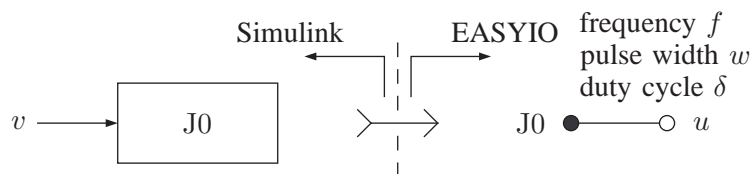
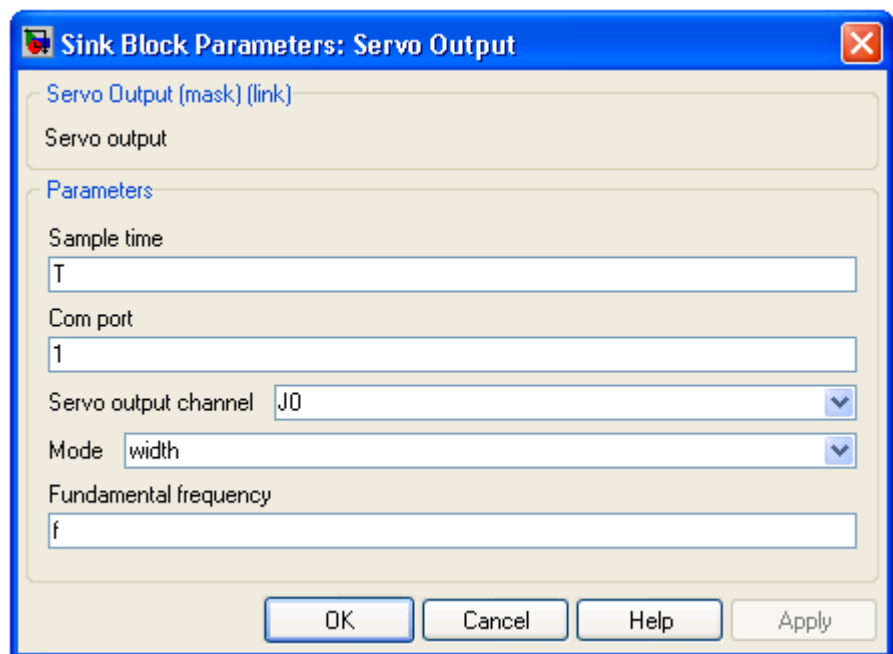
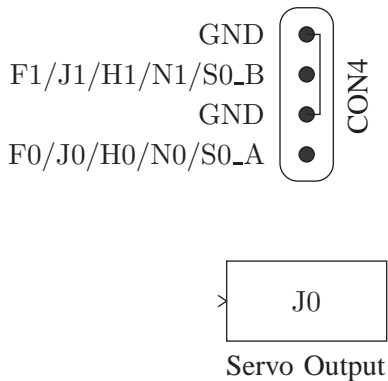


$$\text{width mode} \Rightarrow v \approx \begin{cases} 1/f, & w \geq 1/f \text{ (} u \text{ is high)} \\ w, & 0 < w < 1/f \\ 0, & w \leq 0 \text{ (} u \text{ is low)} \end{cases}$$

$$\text{duty mode} \Rightarrow v \approx \begin{cases} 1, & \delta \geq 1 \text{ (} u \text{ is high)} \\ \delta, & 0 < \delta < 1 \\ 0, & \delta \leq 0 \text{ (} u \text{ is low)} \end{cases}$$

10. Servo Output

- 2 servo output channels J0 – J1
- Block input: pulse width or duty cycle of digital signal
- Board output: 0 – 5 V digital signal
- Resolution: 16 bit
- Frequency range: $7.0287 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$
- $2.1710 \mu\text{s}$ maximum pulse width interpolation error and $2.1710 \times 10^{-6} f$ maximum duty cycle interpolation error (f is the desired output frequency)

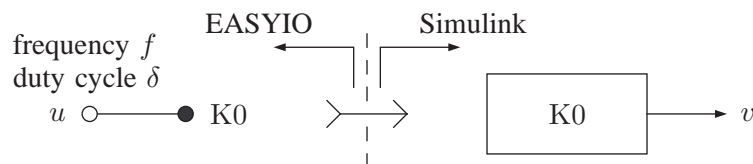
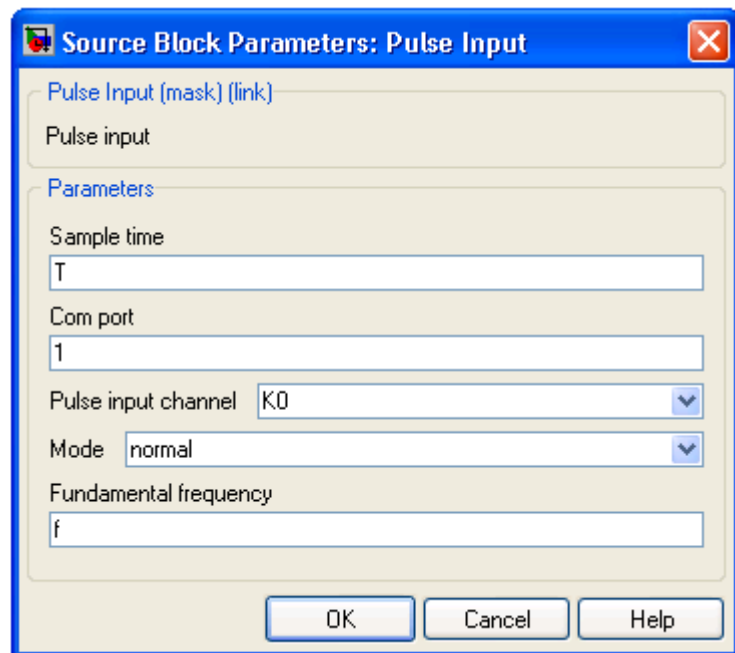
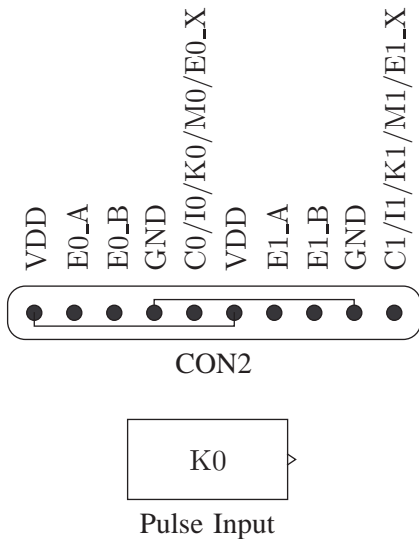


$$\text{width mode} \Rightarrow w \approx \begin{cases} 1/f \text{ (} u \text{ is high)}, & v \geq 1/f \\ v, & 0 < v < 1/f \\ 0 \text{ (} u \text{ is low)}, & v \leq 0 \end{cases}$$

$$\text{duty mode} \Rightarrow \delta \approx \begin{cases} 1 \text{ (} u \text{ is high)}, & v \geq 1/f \\ v, & 0 < v < 1/f \\ 0 \text{ (} u \text{ is low)}, & v \leq 0 \end{cases}$$

11. Pulse Input

- 2 pulse input channels K0 – K1
- Board input: 0 – 5 V digital signal
- Block output: normal or shifted duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $449.8360 \text{ Hz} \leq f \leq 115156.25 \text{ Hz}$
- $33.9213 \times 10^{-9} f$ maximum normal duty cycle quantization error and $67.8426 \times 10^{-9} f$ maximum shifted duty cycle quantization error (f is the actual input frequency)

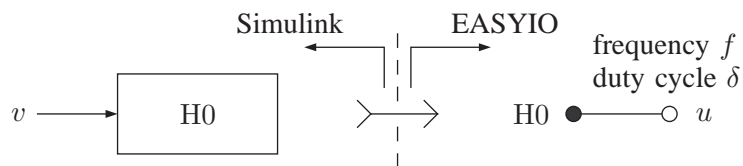
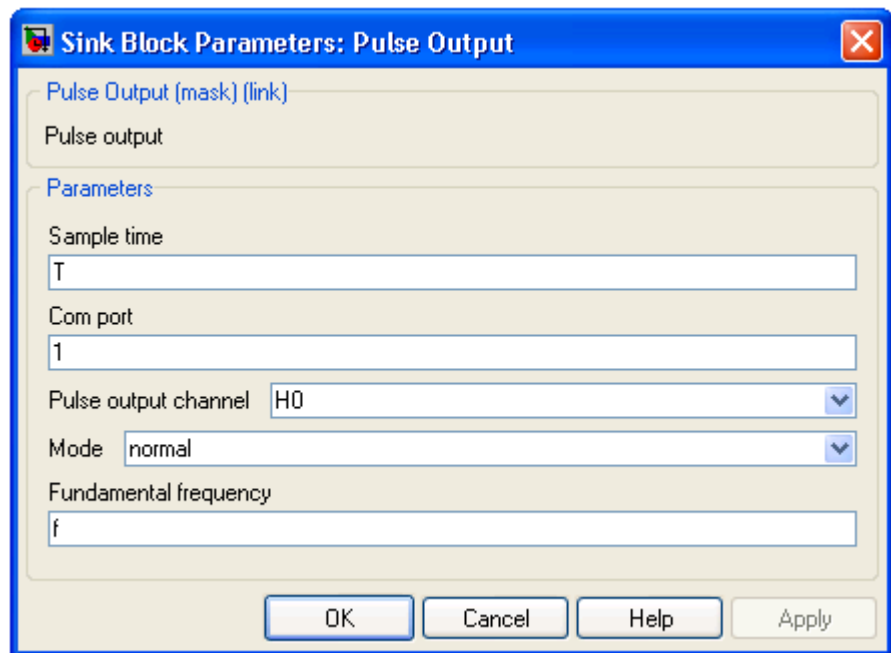
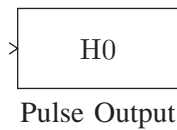
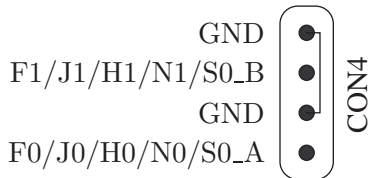


$$\text{normal mode} \Rightarrow v \approx \begin{cases} 1, & \delta \geq 1 \text{ (} u \text{ is high)} \\ \delta, & 0 < \delta < 1 \\ 0, & \delta \leq 0 \text{ (} u \text{ is low)} \end{cases}$$

$$\text{shifted mode} \Rightarrow v \approx \begin{cases} +1, & \delta \geq 1 \text{ (} u \text{ is high)} \\ 2\delta - 1, & 0 < \delta < 1 \\ -1, & \delta \leq 0 \text{ (} u \text{ is low)} \end{cases}$$

12. Pulse Output

- 2 pulse output channels H0 – H1
- Block input: normal or shifted duty cycle of digital signal
- Board output: 0 – 5 V digital signal
- Resolution: 16 bit
- Frequency range: $449.8360 \text{ Hz} \leq f \leq 115156.25 \text{ Hz}$
- $33.9213 \times 10^{-9} f$ maximum normal duty cycle interpolation error and $67.8426 \times 10^{-9} f$ maximum shifted duty cycle interpolation error (f is the desired output frequency)

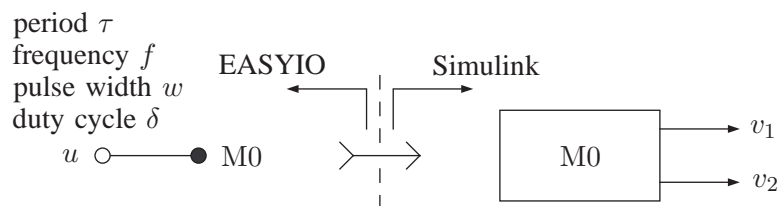
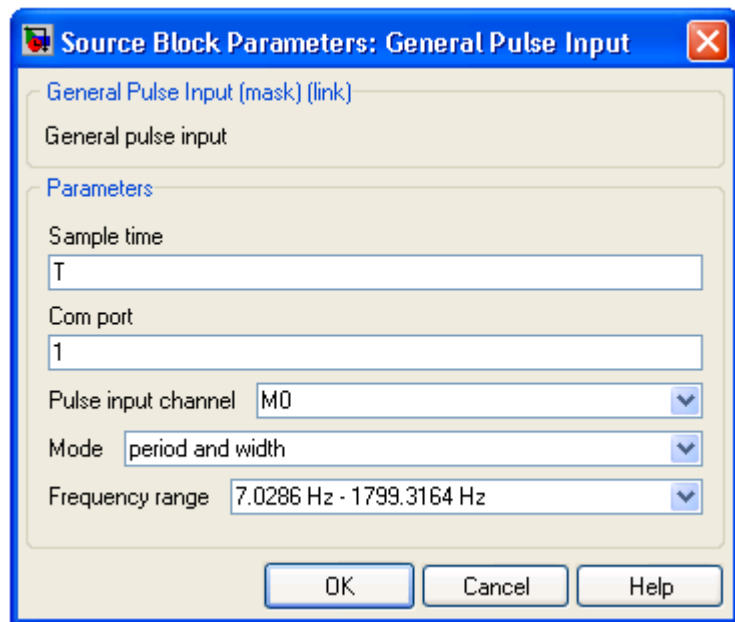
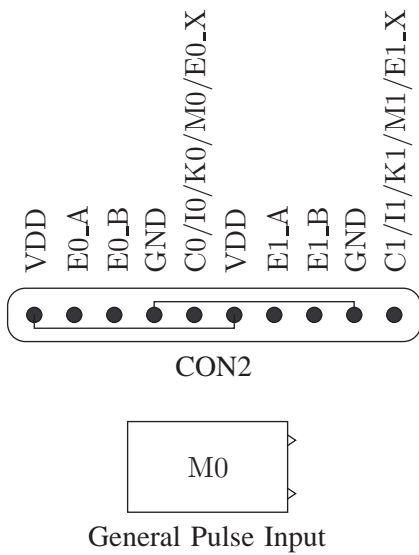


$$\text{normal mode} \Rightarrow \delta \approx \begin{cases} 1 (u \text{ is high}), & v \geq 1 \\ v, & 0 < v < 1 \\ 0 (u \text{ is low}), & v \leq 0 \end{cases}$$

$$\text{shifted mode} \Rightarrow \delta \approx \begin{cases} 1 (u \text{ is high}), & v \geq +1 \\ v/2 + 1/2, & -1 < v < +1 \\ 0 (u \text{ is low}), & v \leq -1 \end{cases}$$

13. General Pulse Input

- 2 general pulse input channels M0 – M1
- Board input: 0 – 5 V digital signal
- Block output: period or frequency and pulse width or duty cycle of digital signal
- Resolution: 16 bit
- Frequency range: $7.0287 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$ or $449.8360 \text{ Hz} \leq f \leq 115156.25 \text{ Hz}$
- $2.1710 \mu\text{s}$ or 33.9213 ns maximum period quantization error and $f - 460625/\lfloor 460625/f \rfloor \text{ Hz}$ or $f - 29480000/\lfloor 29480000/f \rfloor \text{ Hz}$ maximum frequency quantization error (f is the actual input frequency)
- $2.1710 \mu\text{s}$ or 33.9213 ns maximum pulse width quantization error and $2.1710 \times 10^{-6} f$ or $33.9213 \times 10^{-9} f$ maximum duty cycle quantization error (f is the actual input frequency)



$$\begin{aligned} \text{period and width mode} \quad \Rightarrow \quad v_1 &\approx \begin{cases} 2.2230 \times 10^{-3}\kappa, & \tau \geq 2.2230 \times 10^{-3}\kappa \\ \tau, & 8.6839 \times 10^{-6}\kappa < \tau < 2.2230 \times 10^{-3}\kappa \\ 8.6839 \times 10^{-6}\kappa, & \tau \leq 8.6839 \times 10^{-6}\kappa \end{cases} \\ v_2 &\approx \begin{cases} 1/f, & w \geq 1/f \text{ (} u \text{ is high)} \\ w, & 0 < w < 1/f \\ 0, & w \leq 0 \text{ (} u \text{ is low)} \end{cases} \end{aligned}$$

$$\begin{aligned} \text{period and duty mode} \quad \Rightarrow \quad v_1 &\approx \begin{cases} 2.2230 \times 10^{-3}\kappa, & \tau \geq 2.2230 \times 10^{-3}\kappa \\ \tau, & 8.6839 \times 10^{-6}\kappa < \tau < 2.2230 \times 10^{-3}\kappa \\ 8.6839 \times 10^{-6}\kappa, & \tau \leq 8.6839 \times 10^{-6}\kappa \end{cases} \\ v_2 &\approx \begin{cases} 1, & \delta \geq 1 \text{ (} u \text{ is high)} \\ \delta, & 0 < \delta < 1 \\ 0, & \delta \leq 0 \text{ (} u \text{ is low)} \end{cases} \end{aligned}$$

$$\begin{aligned} \text{frequency and width mode} \quad \Rightarrow \quad v_1 &\approx \begin{cases} 115156.25/\kappa, & f \geq 115156.25/\kappa \\ f, & 449.8360/\kappa < f < 115156.25/\kappa \\ 449.8360/\kappa, & f \leq 449.8360/\kappa \end{cases} \\ v_2 &\approx \begin{cases} 1/f, & w \geq 1/f \text{ (} u \text{ is high)} \\ w, & 0 < w < 1/f \\ 0, & w \leq 0 \text{ (} u \text{ is low)} \end{cases} \end{aligned}$$

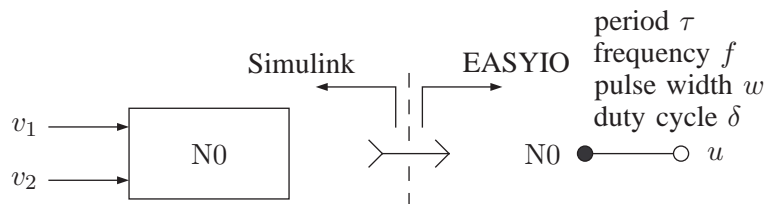
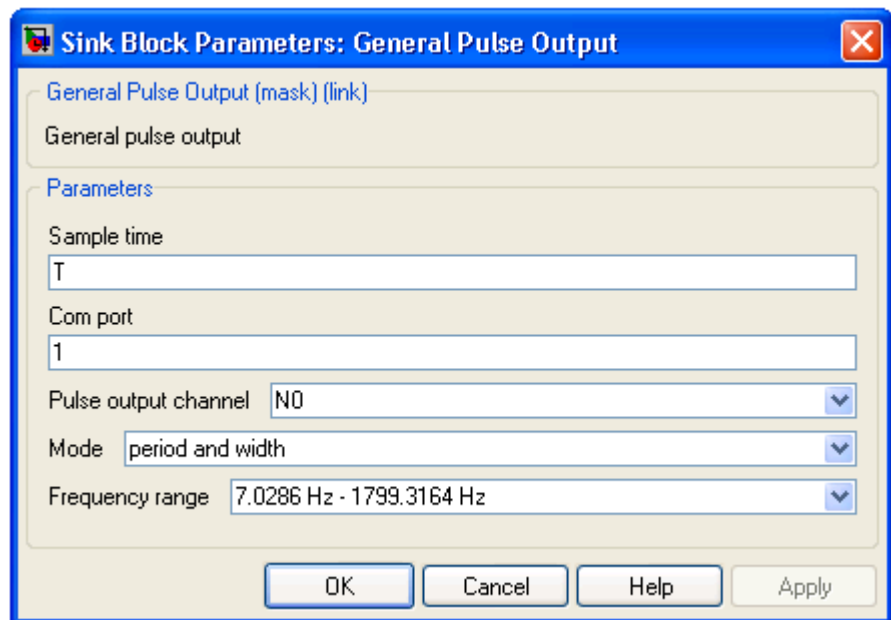
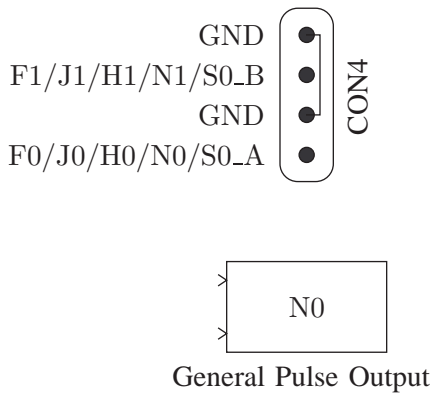
$$\begin{aligned} \text{frequency and duty mode} \quad \Rightarrow \quad v_1 &\approx \begin{cases} 115156.25/\kappa, & f \geq 115156.25/\kappa \\ f, & 449.8360/\kappa < f < 115156.25/\kappa \\ 449.8360/\kappa, & f \leq 449.8360/\kappa \end{cases} \\ v_2 &\approx \begin{cases} 1, & \delta \geq 1 \text{ (} u \text{ is high)} \\ \delta, & 0 < \delta < 1 \\ 0, & \delta \leq 0 \text{ (} u \text{ is low)} \end{cases} \end{aligned}$$

$\kappa = 64$ when 7.0287 Hz – 1799.3164 Hz frequency range selected

$\kappa = 1$ when 449.8360 Hz – 115156.25 Hz frequency range selected

14. General Pulse Output

- 2 general pulse output channels N0 – N1
- Block input: period or frequency and pulse width or duty cycle of digital signal
- Board output: 0 – 5 V digital signal
- Resolution: 16 bit
- Frequency range: $7.0287 \text{ Hz} \leq f \leq 1799.3164 \text{ Hz}$ or $449.8360 \text{ Hz} \leq f \leq 115156.25 \text{ Hz}$
- $2.1710 \mu\text{s}$ or 33.9213 ns maximum period interpolation error and $f - 460625/\lfloor 460625/f \rfloor \text{ Hz}$ or $f - 29480000/\lfloor 29480000/f \rfloor \text{ Hz}$ maximum frequency interpolation error (f is the desired output frequency)
- $2.1710 \mu\text{s}$ or 33.9213 ns maximum pulse width interpolation error and $2.1710 \times 10^{-6} f$ or $33.9213 \times 10^{-9} f$ maximum duty cycle interpolation error (f is the desired output frequency)



$$\begin{aligned} \text{period and width mode} \quad \Rightarrow \quad & \tau \approx \begin{cases} 2.2230 \times 10^{-3}\kappa, & v_1 \geq 2.2230 \times 10^{-3}\kappa \\ v_1, & 8.6839 \times 10^{-6}\kappa < v_1 < 2.2230 \times 10^{-3}\kappa \\ 8.6839 \times 10^{-6}\kappa, & v_1 \leq 8.6839 \times 10^{-6}\kappa \end{cases} \\ & w \approx \begin{cases} 1/f \text{ (} u \text{ is high)}, & v_2 \geq 1/f \\ v_2, & 0 < v_2 < 1/f \\ 0 \text{ (} u \text{ is low)}, & v_2 \leq 0 \end{cases} \end{aligned}$$

$$\begin{aligned} \text{period and duty mode} \quad \Rightarrow \quad & \tau \approx \begin{cases} 2.2230 \times 10^{-3}\kappa, & v_1 \geq 2.2230 \times 10^{-3}\kappa \\ v_1, & 8.6839 \times 10^{-6}\kappa < v_1 < 2.2230 \times 10^{-3}\kappa \\ 8.6839 \times 10^{-6}\kappa, & v_1 \leq 8.6839 \times 10^{-6}\kappa \end{cases} \\ & \delta \approx \begin{cases} 1 \text{ (} u \text{ is high)}, & v_2 \geq 1 \\ v_2, & 0 < v_2 < 1 \\ 0 \text{ (} u \text{ is low)}, & v_2 \leq 0 \end{cases} \end{aligned}$$

$$\begin{aligned} \text{frequency and width mode} \quad \Rightarrow \quad & f \approx \begin{cases} 115156.25/\kappa, & v_1 \geq 115156.25/\kappa \\ v_1, & 449.8360/\kappa < v_1 < 115156.25/\kappa \\ 449.8360/\kappa, & v_1 \leq 449.8360/\kappa \end{cases} \\ & w \approx \begin{cases} 1/f \text{ (} u \text{ is high)}, & v_2 \geq 1/f \\ v_2, & 0 < v_2 < 1/f \\ 0 \text{ (} u \text{ is low)}, & v_2 \leq 0 \end{cases} \end{aligned}$$

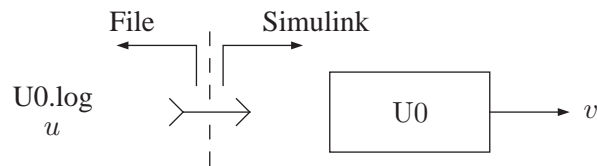
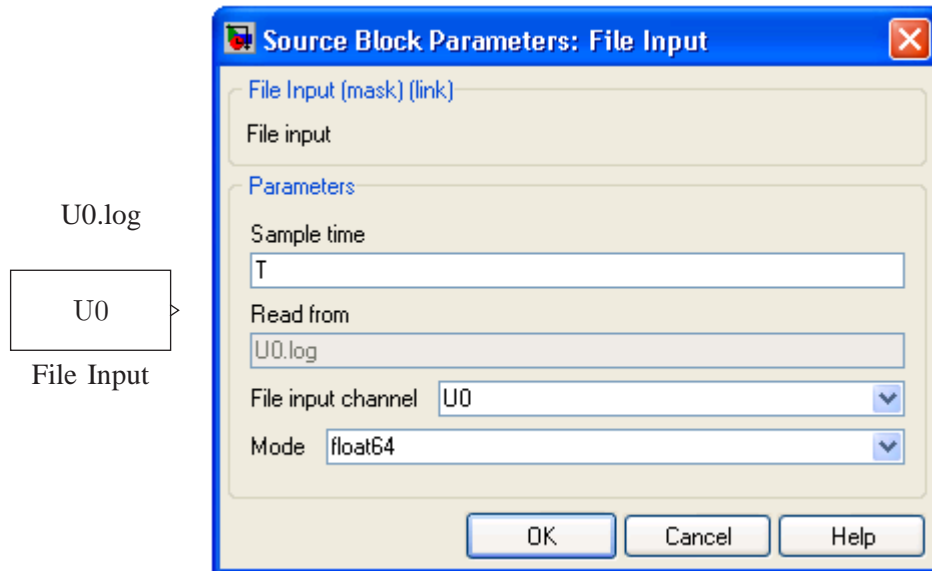
$$\begin{aligned} \text{frequency and duty mode} \quad \Rightarrow \quad & f \approx \begin{cases} 115156.25/\kappa, & v_1 \geq 115156.25/\kappa \\ v_1, & 449.8360/\kappa < v_1 < 115156.25/\kappa \\ 449.8360/\kappa, & v_1 \leq 449.8360/\kappa \end{cases} \\ & \delta \approx \begin{cases} 1 \text{ (} u \text{ is high)}, & v_2 \geq 1 \\ v_2, & 0 < v_2 < 1 \\ 0 \text{ (} u \text{ is low)}, & v_2 \leq 0 \end{cases} \end{aligned}$$

$\kappa = 64$ when 7.0287 Hz – 1799.3164 Hz frequency range selected

$\kappa = 1$ when 449.8360 Hz – 115156.25 Hz frequency range selected

15. File Input

- 8 file input channels U0 – U7
- Input file: raw data in float64 or int16 format
- Block output: signal read from file

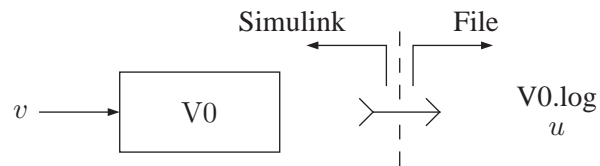
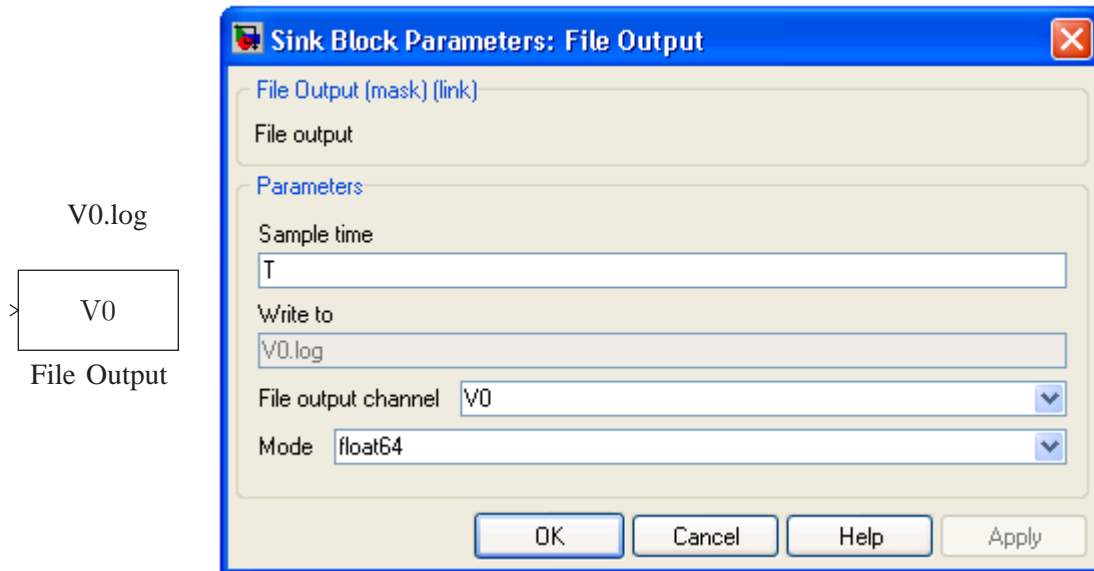


float64 mode $\Rightarrow v = u$ (float64 format)

int16 mode $\Rightarrow v = u$ (int16 format)

16. File Output

- 8 file output channels V0 – V7
- Block input: signal to be written to file
- Output file: raw data in float64 or int16 format

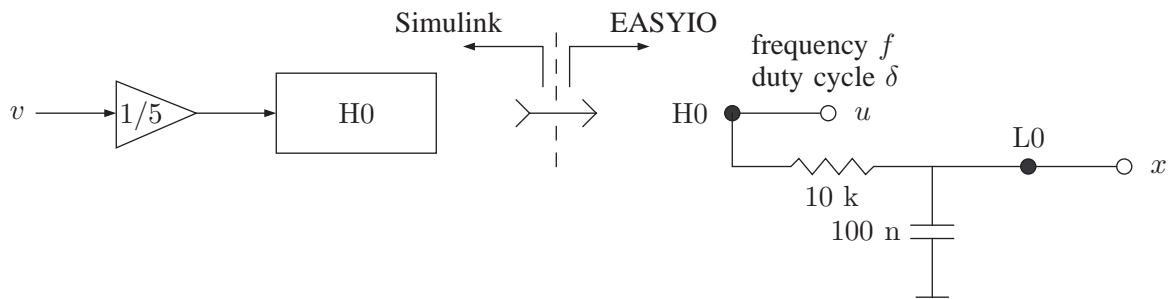


float64 mode $\Rightarrow u = v$ (float64 format)

int16 mode $\Rightarrow u = v$ (int16 format)

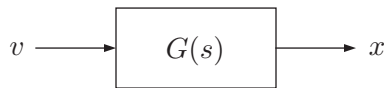
17. Filtered Pulse Output

- 2 filtered pulse output channels L0 – L1
- Board output: 0 – 5 V analog signal
- Bandwidth: 159.1549 Hz
- Filtered pulse outputs can be used as analog outputs



lowpass equivalent of $u \approx \delta 5$

$$f \gg 159.1549 \text{ Hz and H0 in normal mode} \Rightarrow x \approx \begin{cases} 5, & v \geq 5 \\ v, & 0 < v < 5 \\ 0, & v \leq 0 \end{cases}$$

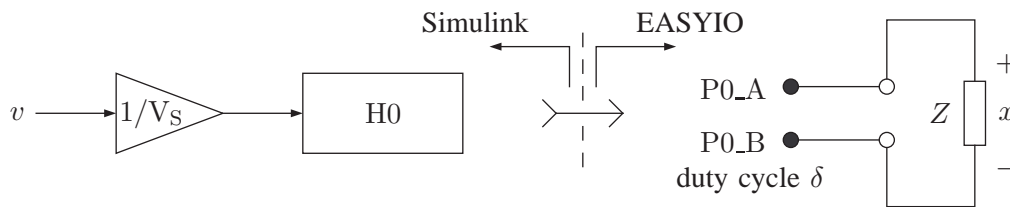


first harmonic (fundamental component) distortion $\eta \approx 20/\pi/\sqrt{1 + (0.002\pi f)^2} \text{ V}$

$$\eta \ll 1 \Rightarrow G(s) = \frac{X(s)}{V(s)} \approx \frac{1}{0.001s + 1}$$

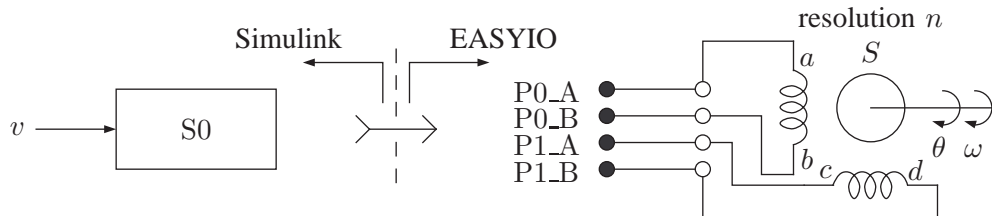
18. H-bridge Power Output

- 2 H-bridge power output channels P0 – P1 with power outputs P0_A, P0_B – P1_A, P1_B
- Board output: $0 - V_S$ V digital power signals (V_S is the power supply voltage)
- Capacity: 5 A
- H-bridge power outputs can be used as power amplifiers to drive heavy loads and stepper motors



lowpass equivalent of $x \approx (2\delta - 1)V_S$

H0 in shifted mode \Rightarrow lowpass equivalent of $x \approx \begin{cases} +V_S, & v \geq +V_S \\ v, & -V_S < v < +V_S \\ -V_S, & v \leq -V_S \end{cases}$









S0 in position mode $\Rightarrow \theta \approx v$

S0 in velocity mode $\Rightarrow \omega \approx v$

19. Sampling Rate

$$\begin{array}{l} \text{number of input channels } n_i \leq 64 \\ \text{number of output channels } n_o \leq 64 \end{array} \Rightarrow \text{sampling rate } f = \frac{1}{T} \leq 1024$$

20. Usage

- Set up the real-time control board with the desired external connections and construct a Simulink model with the desired blocks.
- Define the sample time T ($T = 1/f$, where f is the sampling rate) and the stop time S at the command prompt in the Matlab command window.
- Build the model by clicking on “Tools → Real-Time Workshop → Build Model...” or by pressing Ctrl+B.
- Click on the “Connect to target” button  to connect the board to the model and then click on the “Start real-time code” button  to run the model.
- Click on the “Stop real-time code” button  to stop the model or click on the “Disconnect from target” button  to disconnect the model from the board.
- If the real-time execution is terminated by clicking on the “Stop real-time code” button , the model can be modified, rebuilt and rerun by following the above steps again.
- If, however, the real-time execution is terminated by clicking on the “Disconnect from target” button , the board must be reset before rerunning the model even without any modification since the code is still running on the real-time board.

21. Guidelines

- Refer to the examples that come with the platform for setting up the configuration parameters under “Simulation → Configuration Parameters...” for your model.
- Refer to the Matlab help files for setting up the configuration parameters under “Tools → External Mode Control Panel...” for your model.
- Refer to the Real-Time Windows Target help files for setting up the “Scope parameters” for external data collection.
- Confine all your project files to the EASYIO installation directory and make sure that the “Current Directory” of Matlab is your EASYIO installation directory.
- Make sure that the com port number of each EASYIO block (default is 1) matches with the com port you are using.
- Rebuild your model whenever you make any changes in the parameters of the EASYIO blocks in your model (even when Matlab does not warn you to do so).
- Capture inputs, frequency outputs, sensor inputs, servo outputs, pulse inputs, pulse outputs, general pulse inputs and general pulse outputs can not use the same channel number when used together in the same Simulink model.
- Some inputs and outputs are multiplexed and can not be used together (refer to the User Guide to determine the multiplexed inputs and outputs, and their priority).
- All relevant physical quantities (board and block inputs, outputs and parameters) cited in this document are in SI units for convenience.
- The given quantization and interpolation errors are based on the nominal values of components used on the EASYIO board and are provided only for reference purpose (not guaranteed).
- Do not excessively load (actively or passively) the inputs and outputs of the board beyond their normal operating ranges.
- Refer to the data sheets of the components used on the board for their absolute maximum ratings and safe operating areas.

22. Applications

- Real-time signal analysis, synthesis, processing and visualization
- Parameter tuning and optimization
- Modeling, analysis and design of control systems
- Real-time control
- Hardware-in-the-loop simulation
- Real-time rapid control prototyping
- Teaching concepts and carrying out experiments in signals and systems labs
- Real-time data acquisition

23. Specifications

- Power supply: 6 – 15 V, minimum 0.15 A, regulated, (VPS is + and GND is –)
- Interface: 115200 baud, 8 bit data, no parity, 1 stop bit
- Analog inputs: A0 – A7, 0 – 5 V analog, 12 bit resolution
- Analog outputs: B0 – B1, 0 – 5 V analog, 12 bit resolution
- Digital inputs: D0_d0 – D0_d7, 0 – 5 V digital, 8 lines
- Digital outputs: G0_g0 – G0_g7, 0 – 5 V digital, 8 lines
- Capture inputs: C0 – C1, 0 – 5 V digital, 16 bit resolution
- Frequency outputs: F0 – F1, 0 – 5 V digital, 16 bit resolution
- Encoder inputs: E0_A, E0_B, E0_X – E1_A, E1_B, E1_X, 0 – 5 V digital, 16 bit resolution
- Stepper outputs: S0_A – S0_B, 0 – 5 V digital, 16 bit resolution
- Sensor inputs: I0 – I1, 0 – 5 V digital, 16 bit resolution
- Servo outputs: J0 – J1, 0 – 5 V digital, 16 bit resolution
- Pulse inputs: K0 – K1, 0 – 5 V digital, 16 bit resolution
- Pulse outputs: H0 – H1, 0 – 5 V digital, 16 bit resolution
- General pulse inputs: M0 – M1, 0 – 5 V digital, 16 bit resolution
- General pulse outputs: N0 – N1, 0 – 5 V digital, 16 bit resolution
- File inputs: U0 – U7, internal, 16/64 bit resolution
- File outputs: V0 – V7, internal, 16/64 bit resolution
- Filtered pulse outputs: L0 – L1, 0 – 5 V analog
- H-bridge power outputs: P0_A, P0_B – P1_A, P1_B, 0 – (supply voltage) V digital, 5 A
- Voltage regulator output: VDD, 5 V, 0.25 A, regulated power supply
- Ground: GND, 0 V
- Sampling rate: up to 1024 Hz
- Size: 10.16 cm × 7.62 cm
- Weight: 43.9 g

24. Requirements

- PC with Windows XP or later and an available USB port
- Matlab R2007b or later with Simulink, Real-Time Workshop (Matlab Coder and Simulink Coder) and Real-Time Windows Target (Simulink Desktop Real-Time)
- EASYIO hardware (real-time control board) 2.1 or later
- EASYIO software 2.1 or later
- USB-to-serial converter cable
- Power supply (regulated, 6 – 15 V and at least 0.15 A)

25. Absolute Maximum Ratings

- Power supply voltage: minimum 3 V, maximum 16 V
- Each analog, digital, capture, encoder, sensor, pulse and general pulse input: minimum -0.3 V, maximum $+5.3$ V
- Each analog, digital, frequency, stepper, servo, pulse and general pulse output: minimum -25 mA, maximum $+25$ mA
- Each filtered pulse output: minimum -25 mA, maximum $+25$ mA
- Each H-bridge power output: minimum -5 A, maximum $+5$ A
- Voltage regulator output: maximum 0.5 A (total)
- Total current from/into all inputs and outputs (except power supply, voltage regulator and H-bridges): minimum -200 mA, maximum $+200$ mA
- Operating ambient temperature: minimum 10 °C, maximum 50 °C